Electrical Engr

PROPOSAL NUMBER: 99- 4 1 8

CURRICULUM PROPOSAL FORM

**DEADLINES:*
REGULAR COURSE PROPOSALS: OCTOBER 23, 1998 FOR FALL, 1999 AND FEBRUARY 19, 1999 FOR SPRING, 2000
SHORT-TERM COURSE PROPOSALS: DECEMBER 11, 1998 FOR FALL, 1999 AND MARCH 26, 1998 FOR SPRING 2000

PROPOSAL TITLE: DIGITAL DESIGN w/ VHDL

SPONSOR/S: T. Schulz & ECE Curr. Comm.

DEPARTMENT: ENGINEERING 0909.483

CHECK ALL THAT APPLY:
X UNDERGRADUATE _____GRADUATE

COLLEGE: ENGINEERING
If LAS: _____History/Humanities
_____ Math/Sciences
_____Social/Behavioral Sciences

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TYPE OF PROPOSAL *(Check ALL that Apply)*

_____General Education
___*New Course in* _____*Bank*
___*Existing course, Add To* _____*Bank*
___*Multicultural/Global Designation*
___*Writing Intensive Designation*

_____ New Minor/Concentration/Specialization
_____ New Major/Degree Program
_____ Short Term Course Proposal

___X___ New Course (NOT Gen. Ed.)
_____ Name Change (Dept., School, Major)
_____Changes in Degree Requirements
____*Changes Involve Gen. Ed. requirements*

_____Minor Changes to Existing Courses
_____ *Course is NOT General Education*
_____ *Course IS General Education*

DEPARTMENT
(SIGNATURE INDICATES APPROVAL)

Ravi Prakash Ramachandran 03/09/99
DEPT. CURRICULUM CHAIR / DATE

DEPT. CHAIRPERSON / DATE 3/9/99

COLLEGE CURRICULUM COMMITTEE
DATE OF OPEN HEARING (if necessary) 4/20/99

X APPROVED

----- NOT APPROVED
Comments:

Robert P. Hoskitt 4/20/99
SIGNATURE DATE

ACADEMIC DEAN (& GRADUATE DEAN, for New Graduate Programs Only)

✓ APPROVED

----- NOT APPROVED
Comments:

3/9/99
SIGNATURE (Academic Dean) DATE

SIGNATURE (Graduate Dean) DATE

UNIVERSITY CURRICULUM COMMITTEE

DATE OF OPEN HEARING (if necessary) 4/20/99 (college level)

---- APPROVED

----- NOT APPROVED

Comments:

Annette Reese 4/7/99
SIGNATURE DATE

SENATE

Date announced at Senate 4/30/99

Voted upon at Senate: _____ Approved _____ Not Approved Date: _____

EXECUTIVE VICE PRESIDENT/PROVOST

_____APPROVED

_____NOT APPROVED If no, reasons are as follows:

STUDENT CREDIT HOURS _____ FACULTY LOAD HOURS _____ EQUALIZED CREDIT HOURS _____

OFFICIAL COPY & APPROVAL SHEET FILED (DATE): _____

DATE/SIGNATURE EXECUTIVE VICE PRESIDENT/PROVOST C J Mott 5/24/99

REGISTRAR

DATE APPROVED COURSE DESCRIPTION RECEIVED _____

HEGIS TAXONOMY & COURSE NUMBER ASSIGNED 0909.483

DATE/SIGNATURE OF REGISTRAR Robert A. Kubat 7/6/99

NOTIFICATION FORWARD:

__✓__ SENATE CURRICULUM COMMITTEE CHAIRPERSON

__✓__ DEPARTMENT CHAIRPERSONS

__✓__ ACADEMIC DEAN(S)

__✓__ REGISTRAR

_____ SPONSOR(S)

Course Proposal

1. Details:

a) Course Title:	Digital Design w/ VHDL (0909.483)
b) Sponsor:	Dr. John L. Schmalzel, Electrical and Computer Engineering (ECE) and ECE Curriculum Committee
c) Credit Hours:	3 credit hours
d) Course Level:	Undergraduate (UG)
e) Curricular Effect:	Elective course for UG students
f) Prerequisites:	Digital II (0909.242).
g) Suggested Time/ Scale of Implementation	Fall 1999 and beyond One section
h) Resources	No additional faculty are needed to meet this requirement. Laboratory equipment will be obtained consistent with College of Engineering multi-year budget. No additional library acquisitions will be required.

2. Rationale:

The proposed course is a revision to part of the Engineering Curriculum Proposal approved by the College Senate in December, 1994. The proposed course is consistent with the establishment of the School of Engineering approved by the Board of Trustees in February, 1995.

Digital system design has moved almost exclusively into the domain of descriptive hardware language modeling for system design. VHDL (Very High Speed Integrated Circuit (VHSIC) Hardware Description Language) was originally developed for the military to support advanced IC development for next-generation avionic and munition systems. It has since found widespread acceptance in commercial industry and has spawned similar languages such as Verilog. VHDL not only supports behavioral description of complex digital systems but also supports detailed timing descriptions. This allows very complex systems to be fully modeled. Additional tools are available to allow compilation of VHDL designs into field programmable gate arrays (FPGAs). Other tools support *silicon compilation* that can generate complete IC layouts.

3. Essence of the Course:

a) Objectives:

The proposed course has a number of objectives:

(i) Provide a working knowledge of fundamental constructs of VHDL.

(ii) Provide a structured design methodology appropriate to behavioral modeling of digital systems.

(iii) Explain the relationship between behavioral modeling and verification.

(iv) Provide opportunities to apply didactic principles in a representative complex digital system design applications.

b) Topical Outline:
The content of the course will be designed to reflect current practice.

- Review of logic design fundamentals. Combinational logic; sequential logic. Moore and one-hot state machines. Hazards, timing, setup and hold times.
- Introduction to VHDL. Combinational networks. Modeling F/F's using VHDL processes. Modeling sequential machines. VHDL operators, functions, and procedures. Packages and libraries. VHDL language tools (tools from Xilinx, Mentor Graphics, etc.).
- Design of networks for arithmetic operations. Serial adder with accumulator. Design of a binary multiplier, divider.
- Digital design with state machine (SM) charts. Derivation and realization of SM charts. Example application using SM charts. Relationship between microprogramming and SM charts. Linked state machines.
- VHDL design compilation. Using FPGAs. Comparison of available industry FPGA offerings.
- Floating-point (FP) arithmetic. Floating-point representation. Design and implementation of FP operations.
- Advanced VHDL. Attributes. Transport and inertial delays. Multivalued logic and signal resolution. IEEE-1164 standard logic. Generate statements.
- VHDL models for memories and buses. Static RAM memory. Processor bus models. Memory to bus interfacing.
- Hardware testing and design for testability. Combination and sequential logic testing. Scan Testing. Boundary scan. Built-in Self-Test (BIST). ANSI/IEEE 1149.1.
- VHDL design examples. Communication interface (e.g., UART). Eight-bit microcontroller design.
- Design project.

c) Evaluation and Grading Procedures:

Student grades will be based on projects, examinations, homework, and written and oral technical communication.

d) Course Evaluation:

The proposed course will be evaluated based on student evaluations and critical review by engineering faculty.

e) Texts:

A large number of texts are available. Strong possibilities for this course include:

C.H. Roth, Jr. *Digital System Design Using VHDL*. PWS Publ, 1997.

P.J. Ashenden, *Designer's Guide to VHDL*. Morgan Kaufman, 1995. (A student guide is also available, 1998.)

D.L. Perry, *VHDL, 3rd ed.* McGraw-Hill, 1998. (This is the classic text in the area, although it may not be the best written text for student use.)

4. Results of Consultations:

a) Consulted Departments: Computer Science.

b) Consultants and Consultant Statements:

c) Written Consultations:

5. Additional Supporting Information:

6. Catalog Description:

TITLE: Digital Design with VHDL (ECE 483)

The course uses VHDL to model and simulate digital systems. Specialized features of the language are presented to allow getting optimum results from simulations. Example VHDL applications are explored and a project is used to complement the course.

Prerequisite: Digital II (0909.242)